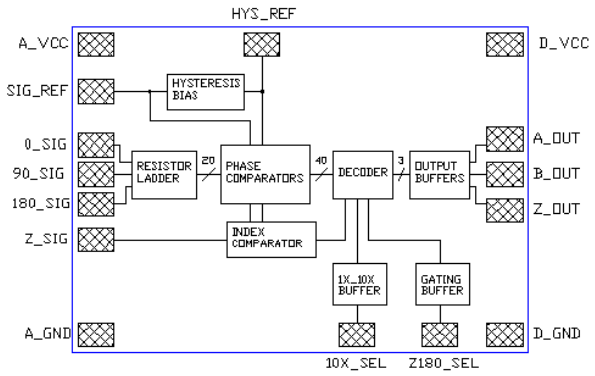
INTERPOLATION DEVICE
(Interpolation factors of 1X or 10X)

ET2110

FEATURES

- Interpolation factor pin selectable (1X/10X)
- Index gating pin selectable (90/180 electrical degrees of interpolated pulse)
- Leading edge of gated index pulse occurs at 270 electrical degrees of analog input cycle, regardless of interpolation factor selected
- Interfaces directly with ET2010 Analog Signal Processor and ET7272 Line Driver
- Single supply operation
- Handles Sine/Cosine inputs from DC to 125KHz
- Sine/Cosine input voltage range 400mVpp to 4Vpp on 2.5VDC reference
- Outputs are NPN Collector with 4K pull-up; sink up to 4mA external load
- Outputs TTL and CMOS compatible



DESCRIPTION

This ET2110 is a monolithic bipolar integrated circuit designed to facilitate increased resolution in optical encoder applications by converting the incoming sine and cosine signals to an interpolated quadrature digital output at 1 or 5 times the input frequency. Please refer to the **Timing Diagram**. The device inputs receive photodiode signals which have been amplified and conditioned to optimize the interpolation function. This conditioning may be obtained from a companion device, the analog signal processor, ET2010. Following interpolation processing by the ET2110, the output signal can be fed into a line driver device, such as the ET7272B, for driving extended loads. Please see the **Application Circuit**.

In addition to processing the data channel information, the ET2110 provides a channel for the index signal which controls the gating of the index pulse relative to the 0° and 90° input waveforms. Index gating is provided to generate a pulse that commences at 270 electrical degrees of the analog input cycle. Width of the index pulse is either 90 or 180 electrical degrees of the interpolated pulse (pin selectable).

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min.	Max.	Units	Comments
Operating Temperature Range	T_A	-40	120	°C	
Storage Temperature Range	T_S	-55	150		
Supply Voltage Range	V_{CC}	4.5	5.5	V	

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ELECTRICAL CHARACTERISTICS

Unless otherwise specified, typical values given at V_{CC}=5V, T_A = 25°C, and V_{IN} = 1.6$V_{(P-P)}$.

Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Analog Supply Current	I_{CCA}	---	15.0	19.0	mA	V_{CC} = 5.5V
Digital Supply Current	I_{CCD}	---	6.0	9.0	mA	V_{CC} = 5.5V
Hysteresis REF Voltage	V_{REF}	2.48	2.53	2.58	V	SIG_REF=2.5V
SIG_REF Input Current, high	I_{SIG_REF}	0	17	50	uA	V_{IN} = 4.0V
Z_SIG Input Current, high	$I_{Z\ SIG}$	0	90	200	µA	V_{IN} = 4.0V
10X Select Input Current, high	I_{10X}	-50	-25	0	uA	V_{IN} = 4.0V
Z_SEL Input Current, high	I_{SEL}	-50	-25	0	uA	V_{IN} = 4.0V
0_SIG, 90_SIG, and 180_SIG	I_{SIG}	-2	---	2	mA	
SIG_REF Input Current, low	I_{SIG_REF0}	-100	-47	0	uA	V_{IN} = 0V
Z_SIG Input Current, low	$I_{Z\ SIG0}$	-500	-350	-100	µA	V_{IN} = 0V
10X Select Input Current, low	I_{10X0}	-200	-125	0	uA	V_{IN} = 0V
Z_SEL Input Current,low	I_{SEL0}	-200	-125	0	uA	V_{IN} = 0V
Low Level Output Voltage, A_OUT, B_OUT, and Z_OUT	V_{OL}	---	---	400	mV	Vcc=4.5V, I_{OL}=4mA
High Level Output Voltage, A_OUT, B_OUT, and Z_OUT	V_{OH}	4.9	---	--	V	V_{CC} = 5.5V, I_{OH} = -100uA
Quadrature Error (1X mode) , A_OUT to B_OUT (leading edges)	E_{1X}	-2	---	2	°e *	Note 3
Quadrature Error (10X mode) , A_OUT to B_OUT (leading edges)	E_{10X}	-20	---	20	°e *	Note 3
Pulse Symmetry (width), in 1X and 10X modes, A_OUT, B_OUT, and Z_OUT	PW_{10X}	-10	---	10	%	
Frequency Response at Digital Outputs	f_{CO}	1000	--	--	KHz	Note 1
Internal Pull-up Resistor	R_{INT}	3.0	--	5.0	KOhm	Note 1

NOTES:

1. This is not a test parameter, but guaranteed by design.
2. Unused inputs should be connected to ground.
3. This symbol represents electrical degrees.

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PIN FUNCTION TABLE

PIN #	PIN NAME	FUNCTION
2	HYSTERESIS_REFERENCE	Intended to be left open.
3	ANALOG_VCC	Voltage supply for analog portion of circuit. Bypass to A_GND.
5	ANALOG _GND	Return for analog supply voltage.
6	SIGNAL_REFERENCE	An input and the DC offset level of the sine wave inputs. Bypass to A_GND.
7,8,9	0_SIG, 90_SIG, 180_SIG	Sine wave inputs. When 0_SIG leads 90_SIG, then A leads B at the quadrature outputs. Amplitude should be about 1.6Vpp.
10	Z_SIG	High impedance input with comparator threshold at 2.5V.
11	Z180_SEL	High impedance input to select width of the index pulse. When >2.5V, Z_OUT= 180/X electrical degrees, gated on B_LOW. When <2.5V, Z_OUT= 90/X electrical degrees, gated on (A_LOW AND B_LOW).
12	10X_SEL	High impedance input to select interpolation factor. When >2.5V, the factor is 10X and when <2.5V the factor is 1X.
13	D_GND	Return for the digital supply voltage.
14,16,18	B_OUT, Z_OUT, A_OUT	NPN open collector with internal 4K pull-up resistor.
20	D_VCC	Voltage supply for the digital portion of circuit. Bypass to D_GND.
15,17,19	n/c	While there is no internal connection, these pins should be tied to D_GND on the PCB to shield against output-output crosstalk.

Application

Please refer also to the block diagram on the following page. The sine and cosine inputs (0_SIG, 90_SIG, 180_SIG) should be in the range of 400mVpp to 4Vpp, with a DC offset of 2.5V . Care must be taken to limit the noise on the analog inputs to avoid spurious signals at the outputs. The hysteresis of the phase comparators is 20mV, and while a large input signal may seem advantageous, it is so only as long as the noise is well below the 20mV level. Therefore, from a practical standpoint, the input levels are often limited to the 1.5Vpp range. The ET2110 accepts the DC offset of the analog signals as an input at the SIG_REF pin. The outputs are NPN collectors with 4K pull-ups. For high-frequency applications, output rise time can be reduced by addition of external pull-up resistors as low as 1.5K, as long as the 4mA limit on external loading is not exceeded.

For applications that use photodiode sensing, ETIC offers the ET2010 Analog Signal Processor for generating sine/cosine signals compatible with the ET2110. Please refer to the Application Circuit, which handles inputs from photodiode sensors and processes them through to line driver outputs.

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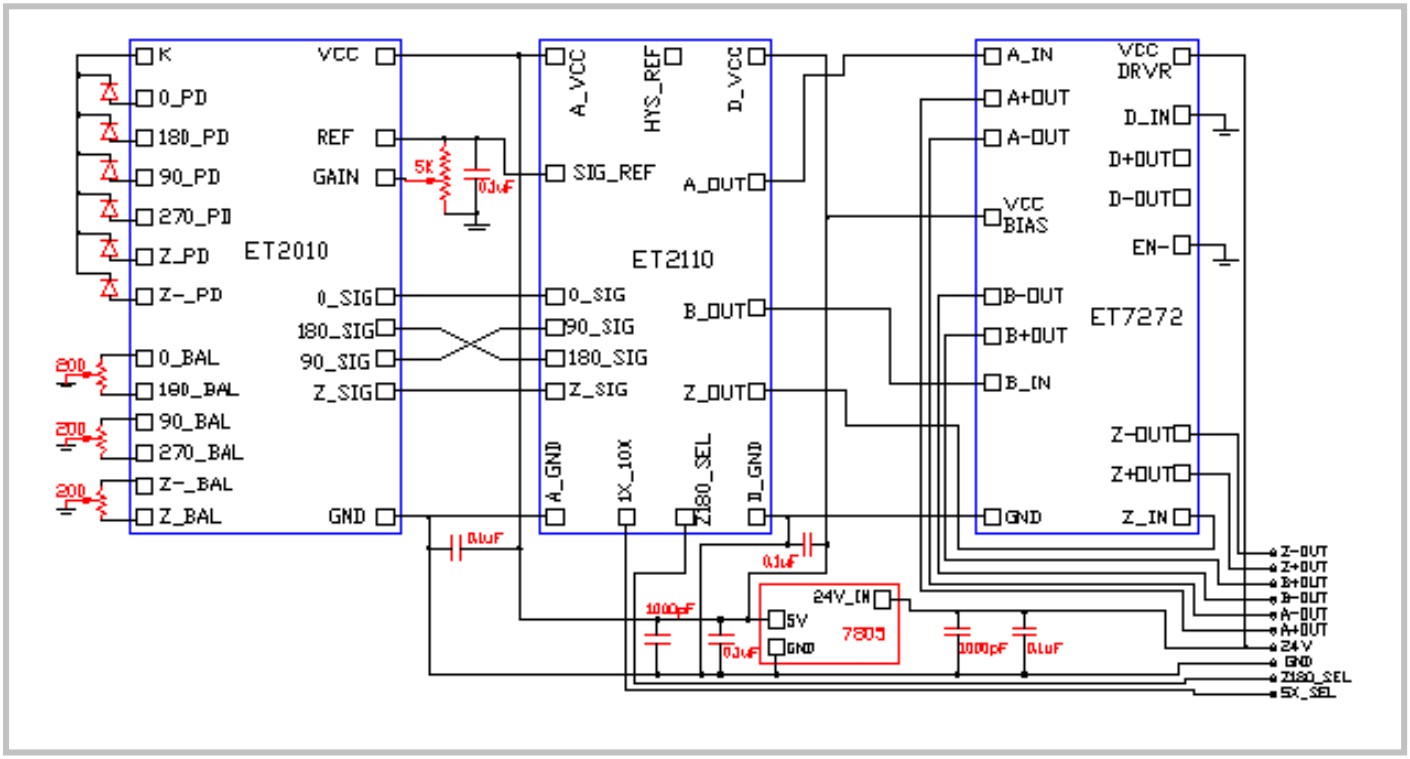

Application Circuit

Disk Optimization

The placement of the index feature on the encoder disk can be optimized, depending on the variety of interpolation factors and index widths that will be used with a given disk. The basic placement for the index pulse would be centered on 0°, and with a width of one cycle (360° electrical). At this point, the 0°_SIG (Sine) is at its positive zero crossing, and the 90°_SIG (Cosine) is at its negative peak.This gives the best manufacturing tolerance for the Z180 pulse in 1X mode, which is the worst case. With this placement, the gated Z pulses from the 2110 will be as shown below in the Timing Diagram. If a disk is to be used in 10X interpolation mode, and with both Z90 and Z180 index gating modes, then the index feature should be centered at 279 degrees of the analog input cycle. If the application is designed uniquely for 10X interpolation in the Z90 mode, the index feature on the disk should be centered at 274.5 degrees. Optimization of the disk in this manner affords a wider margin for misalignment, and can therefore enhance the ease of assembly in volume production.

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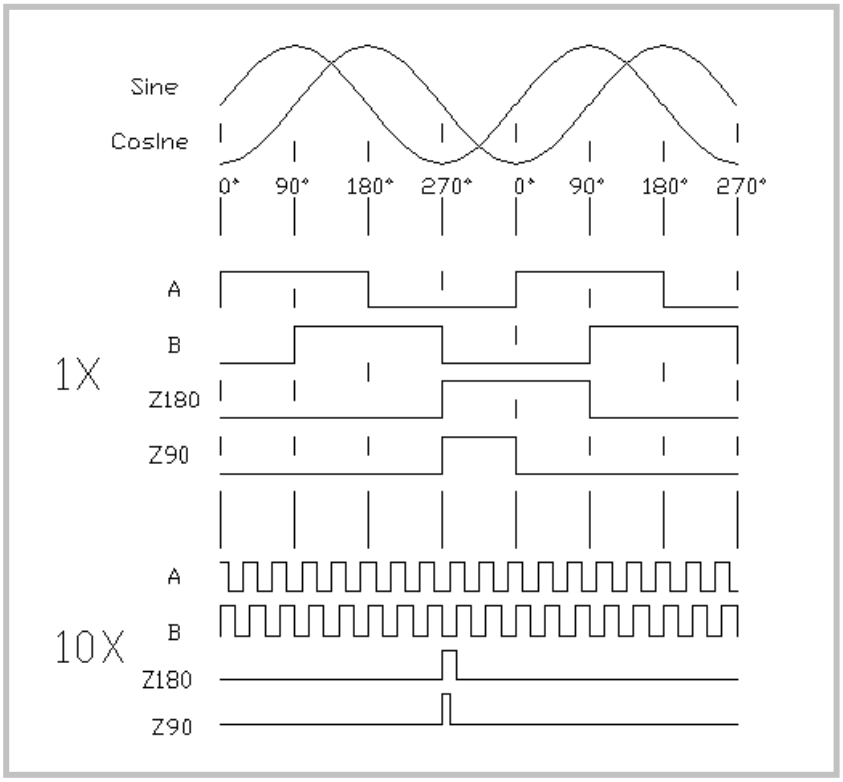
Timing Diagram

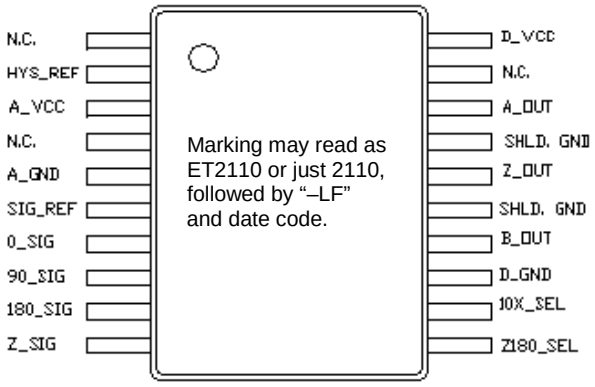


Ordering Information:

PART NUMBER	DESCRIPTION	PACKAGING	MINIMUM ORDER
ET2110 SSOP	20L SSOP (See drawing)	50 per tube	50
ET2110 T&R SCAN	SSOP on Tape & Reel with 100% lead inspection	Reel size & qty per customer PO	500

ET2110 SSOP

Package Drawing for 20L SSOP



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